AMENDMENTS TO THE CLAIMS:

1. (Currently amended) An adaptive equalizer circuit which adds given equalization characteristics to signals ~~inputted~~ input through a transmission path and performs a control such that an equalization error obtained by performing an arithmetic operation based on an obtained output and a given reference value is minimized thus obtaining equalization characteristics,

the improvement being characterized in that the adaptive equalizer circuit ~~has a constitution to change~~ changes the equalization characteristics ~~in which~~ wherein the arithmetic operation of the adaptive equalizer circuit is performed in ~~synchronous~~ synchronization with a signal having a phase different from the reference clock signal of the signal by a 1/2 clock cycle, the synchronization is realized by sampling data at the point of 1/2 clock cycle different from the zero-crossing point of the signal,

and the equalization characteristics are changed by computing the equalization error based on a first output value and said given reference value after a sign of ~~the~~ an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive ~~and said given reference value~~.

2. (Currently amended) An adaptive equalizer circuit according to claim 1, wherein ~~the constitution to change the equalization characteristics is a constitution in which~~ the equalization characteristics of the adaptive equalizer circuit are changed based on the first output value and the first reference value after the sign of the output of the adaptive equalizer circuit is changed from positive to negative, and ~~a first reference value, and~~ the equalization characteristics ~~of the adaptive equalizer circuit~~ are changed based on the first output and the second reference value after the sign

of the output of the adaptive equalizer circuit is changed from negative to positive ~~and a second reference value~~.

3. (Currently amended) An adaptive equalizer circuit according to claim 2, wherein in addition to the change operation of the equalization characteristics of the adaptive equalizer circuit, the adaptive equalizer circuit ~~is constituted such that~~ changes the equalization characteristics of the adaptive equalizer circuit ~~is changed~~ based on the second reference value and the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative ~~and the second reference value~~, and the equalization characteristics ~~of the adaptive equalizer circuit is~~ are changed based on the first reference value and the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from negative to positive ~~and the first reference value~~.

4. (Currently amended) An adaptive equalizer circuit according to claim 1, wherein ~~said constitution which changes the equalization characteristics is a constitution in which~~ the equalization characteristics of the adaptive equalizer circuit are changed based on the first output value and the first reference value after ~~the~~ a sign of ~~the~~ an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive ~~and the first reference value~~, and the equalization characteristics ~~of the adaptive equalizer circuit~~ are changed based on the second reference value and the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive ~~and the second reference value~~.

5. (Original) An adaptive equalizer circuit according to claim 2, wherein the second reference value is set to a value which inverts the sign of the first reference value.

6. (Currently amended) An adaptive equalizer circuit according to claim 1, wherein the adaptive equalizer circuit is operated to sample an input signal with a signal having a phase different from the reference clock signal which is in ~~synchronous~~ synchronization with the input signal by a 1/2 clock cycle, and the equalization characteristics is changed based on the output value of the adaptive equalizer circuit.

7. (Cancelled)

8. (Currently Amended) An adaptive equalizer circuit ~~according to claim 1~~ which adds given equalization characteristics to signals input through a transmission path and performs a control such that an equalization error obtained by performing an arithmetic operation based on an obtained output and a given reference value is minimized thus obtaining equalization characteristics,

the improvement being characterized in that the adaptive equalizer circuit changes the equalization characteristics wherein the arithmetic operation of the adaptive equalizer circuit is performed in synchronization with a signal having a phase different from the reference clock signal of the signal by a 1/2 clock cycle,

and the equalization characteristics are changed by computing the equalization error based on a first output value and said given reference value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive,

wherein the reference values are changed corresponding to the change of threshold values at the time of ~~binarizing~~ digitizing the output of the adaptive equalizer circuit.

9. (Original) An adaptive equalizer circuit according to claim 1, wherein the signals inputted to the adaptive equalizer circuit are signals optically read from a recording medium.